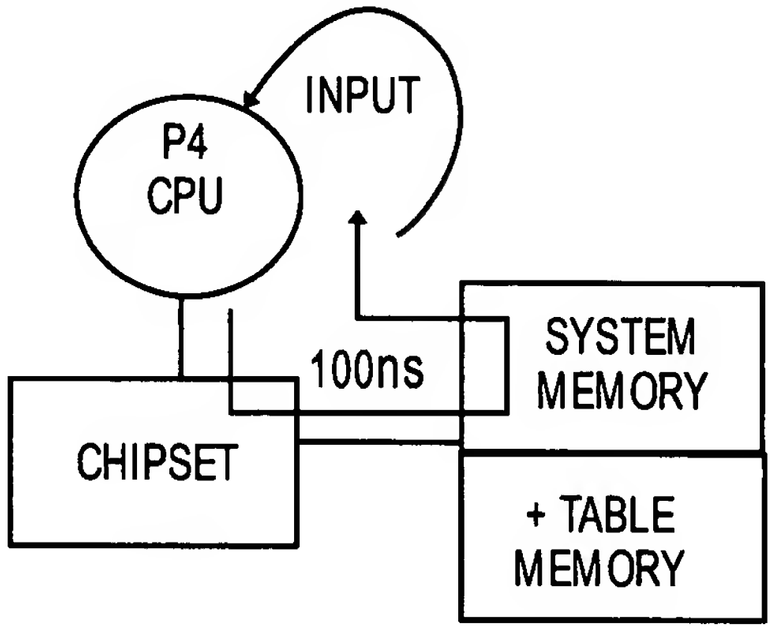
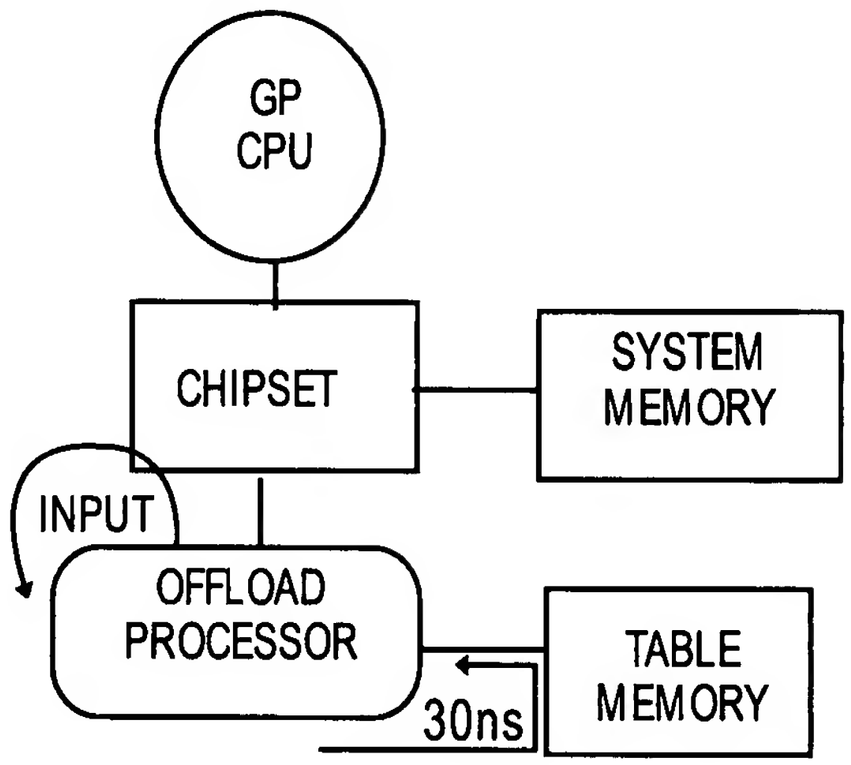
PROPERTIES OF DFA AND NFA TECHNIQUES USED ON CONVENTIONAL MICROPROCESSORS	STORAGE BOUND ON # OF STATES (FOR R CHARACTER REGULAR EXPRESSION)	EVALUATION TIME (FOR N BYTES OF INPUT) [ORDER OF]
DETERMINISTIC FINITE STATE AUTOMATA OR DFA RUNNING ON A GP CPU	2^R (NEEDS VERY LARGE MEMORY)	N MEMORY ACCESS CYCLES
NON-DETERMINISTIC FINITE STATE AUTOMATA NFA RUNNING ON A GP CPU	R	R * N CPU CACHE+BRANCH CYCLES

FIG. 1A

CPU WALKING DFA TABLE IN DRAM



COPROCESSOR CLOSER TO TABLE IN SRAM



PERFORMANCE ON EVALUATING REGULAR EXPRESSIONS ON EVERY BYTE OF INPUT STREAM

1000s OF REs @ 100 Mbps

GIGABYTES OF MEMORY

100s OF REs @ 280 Mbps

100s OF MBs OF SRAM

FIG. 1B

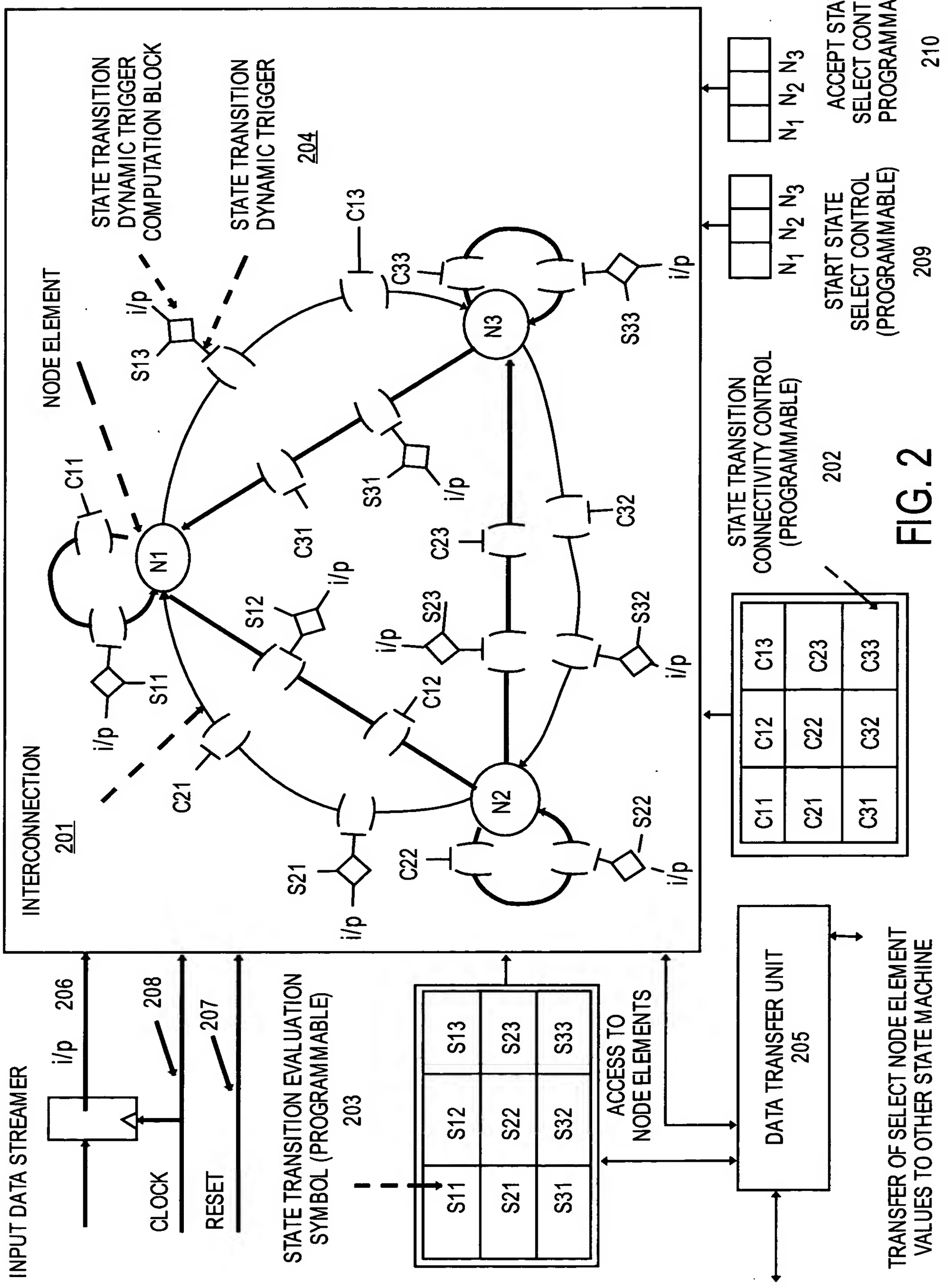

INTERCONNECTION
201
NODE ELEMENT
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION BLOCK
STATE TRANSITION DYNAMIC TRIGGER
204
N1
N2
N3
C11
C12
C13
C21
C22
C23
C31
C32
C33
S11
S12
S13
S21
S22
S23
S31
S32
S33
i/p
START STATE SELECT CONTROL (PROGRAMMABLE)
209
ACCEPT STATE SELECT CONTROL PROGRAMMABLE
210
N_1 N_2 N_3
STATE TRANSITION CONNECTIVITY CONTROL (PROGRAMMABLE)
202
INPUT DATA STREAMER
206
CLOCK
208
RESET
207
STATE TRANSITION EVALUATION SYMBOL (PROGRAMMABLE)
203
ACCESS TO NODE ELEMENTS
DATA TRANSFER UNIT
205
TRANSFER OF SELECT NODE ELEMENT VALUES TO OTHER STATE MACHINE

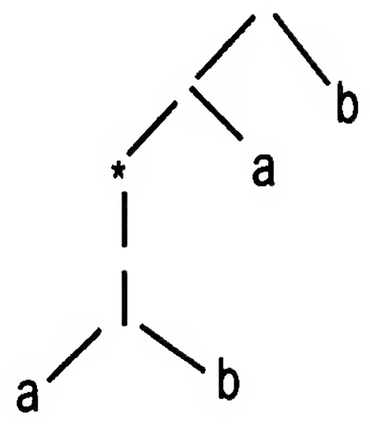
FIG. 2

RE=(alb)* ab

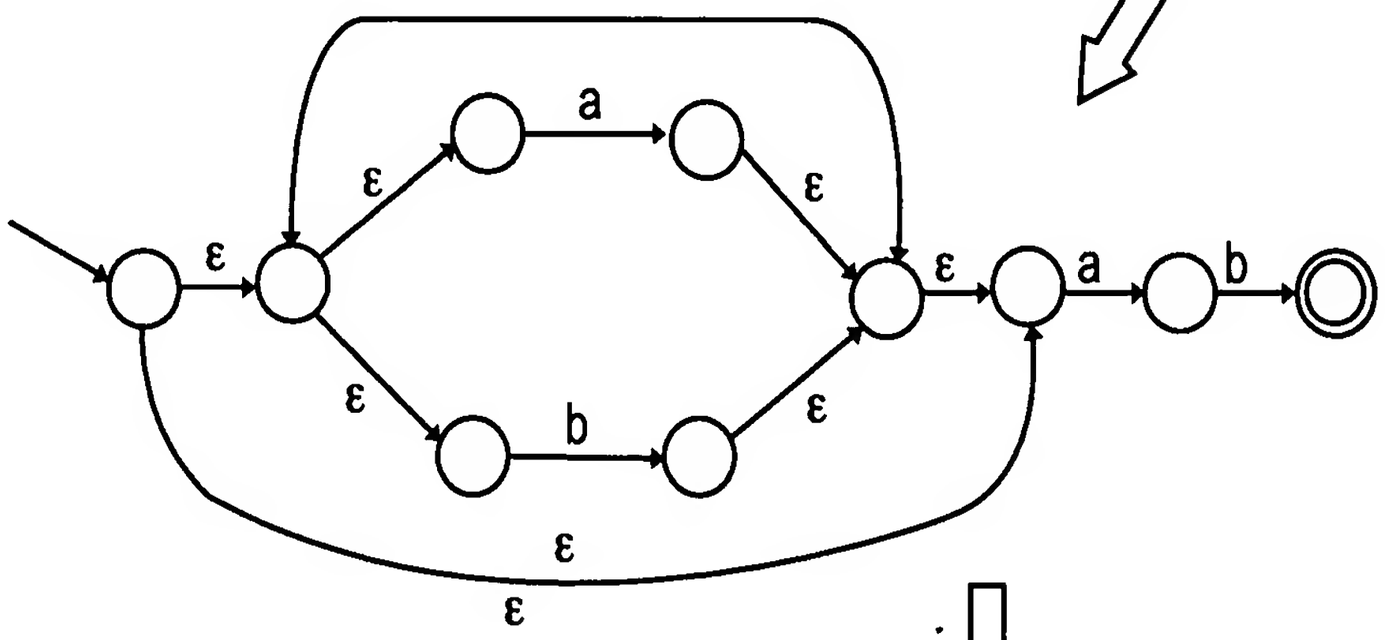
= START STATE

= ACCEPTING STATE

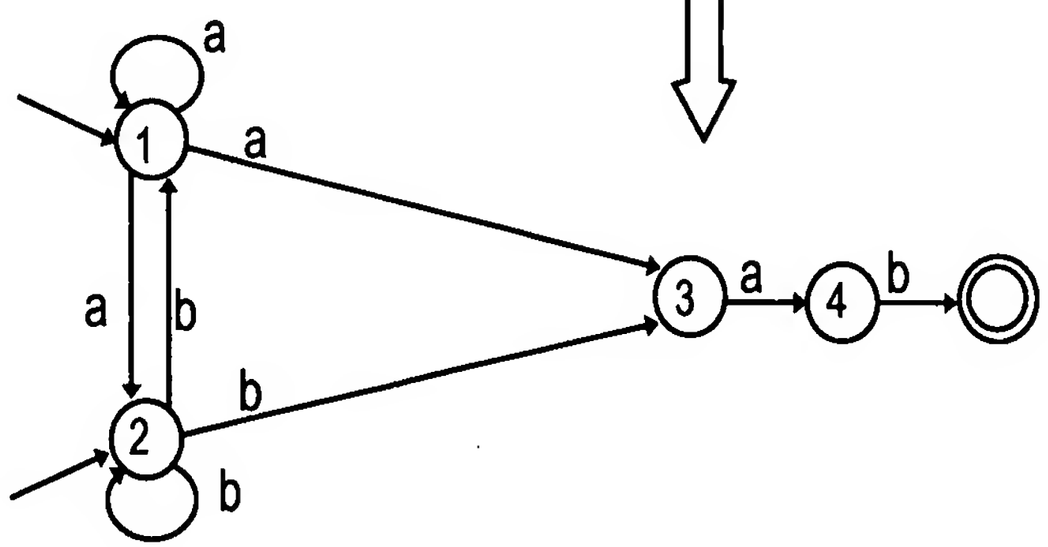
RE PARSE TREE



THOMPSON'S NFA



NFA WITHOUT ε ARCS



FOR RE WITH R CHARS AND 0 OPERATORS

- NFA HAS EPSILON TRANSITIONS (ε). ε IMPLIES A SPECIAL UNCONDITIONAL ZERO-CYCLE STATE TRANSITION
- 2* (R+O)+1 STATES
- R CHARACTER COMPARATORS

FOR RE WITH R CHARS

- R+1 STATES
- MAXIMUM R^2 ARCS
- R CHARACTER COMPARATORS

FIG. 3A

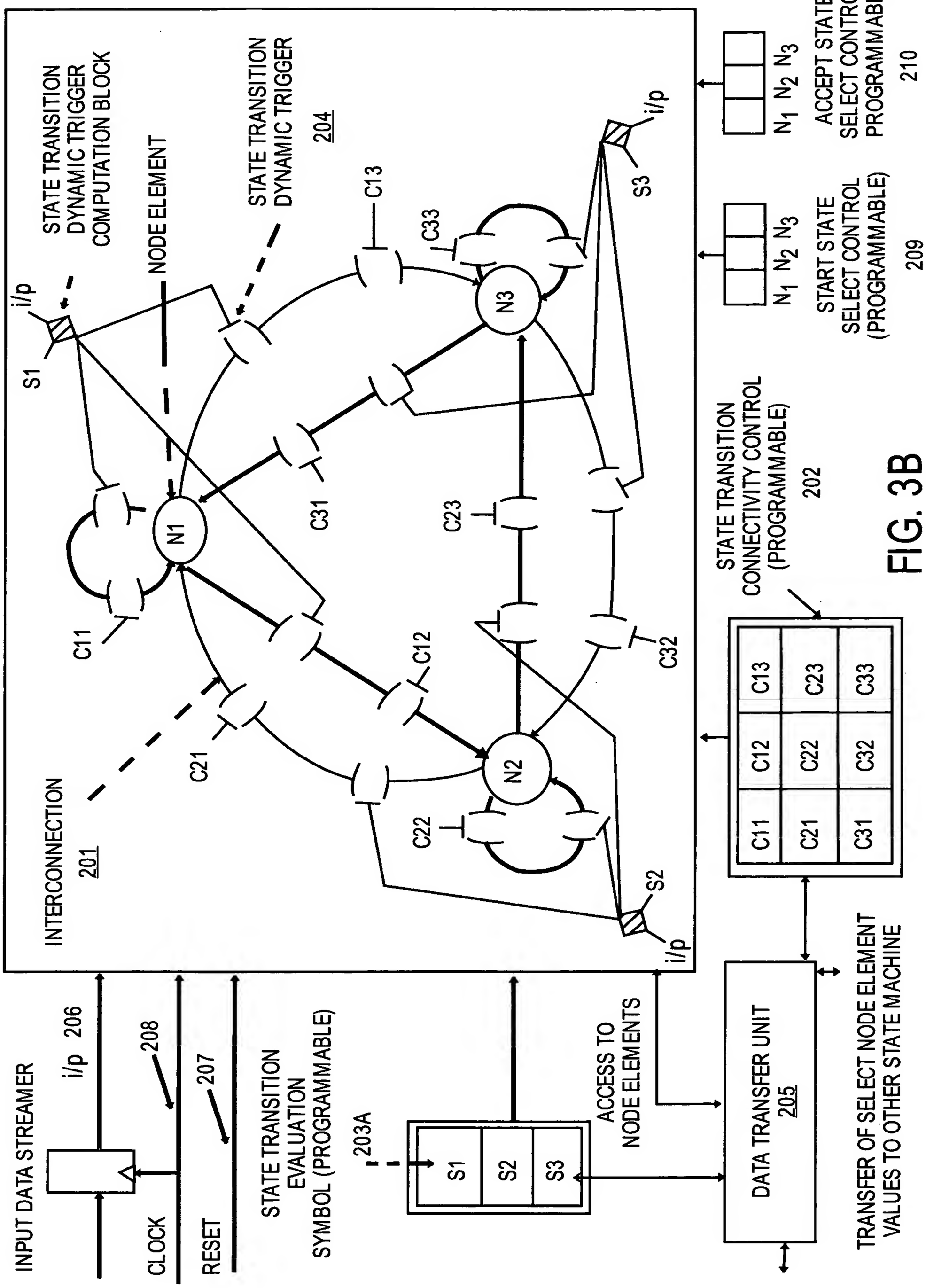

INTERCONNECTION 201
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION BLOCK
NODE ELEMENT
STATE TRANSITION DYNAMIC TRIGGER 204
i/p
S1
S2
S3
N1
N2
N3
C11
C12
C13
C21
C22
C23
C31
C32
C33
START STATE SELECT CONTROL (PROGRAMMABLE) 209
ACCEPT STATE SELECT CONTROL PROGRAMMABLE 210
N_1 N_2 N_3
STATE TRANSITION CONNECTIVITY CONTROL (PROGRAMMABLE) 202
INPUT DATA STREAMER
i/p 206
CLOCK
208
RESET
207
STATE TRANSITION EVALUATION SYMBOL (PROGRAMMABLE)
203A
ACCESS TO NODE ELEMENTS
DATA TRANSFER UNIT 205
TRANSFER OF SELECT NODE ELEMENT VALUES TO OTHER STATE MACHINE

FIG. 3B

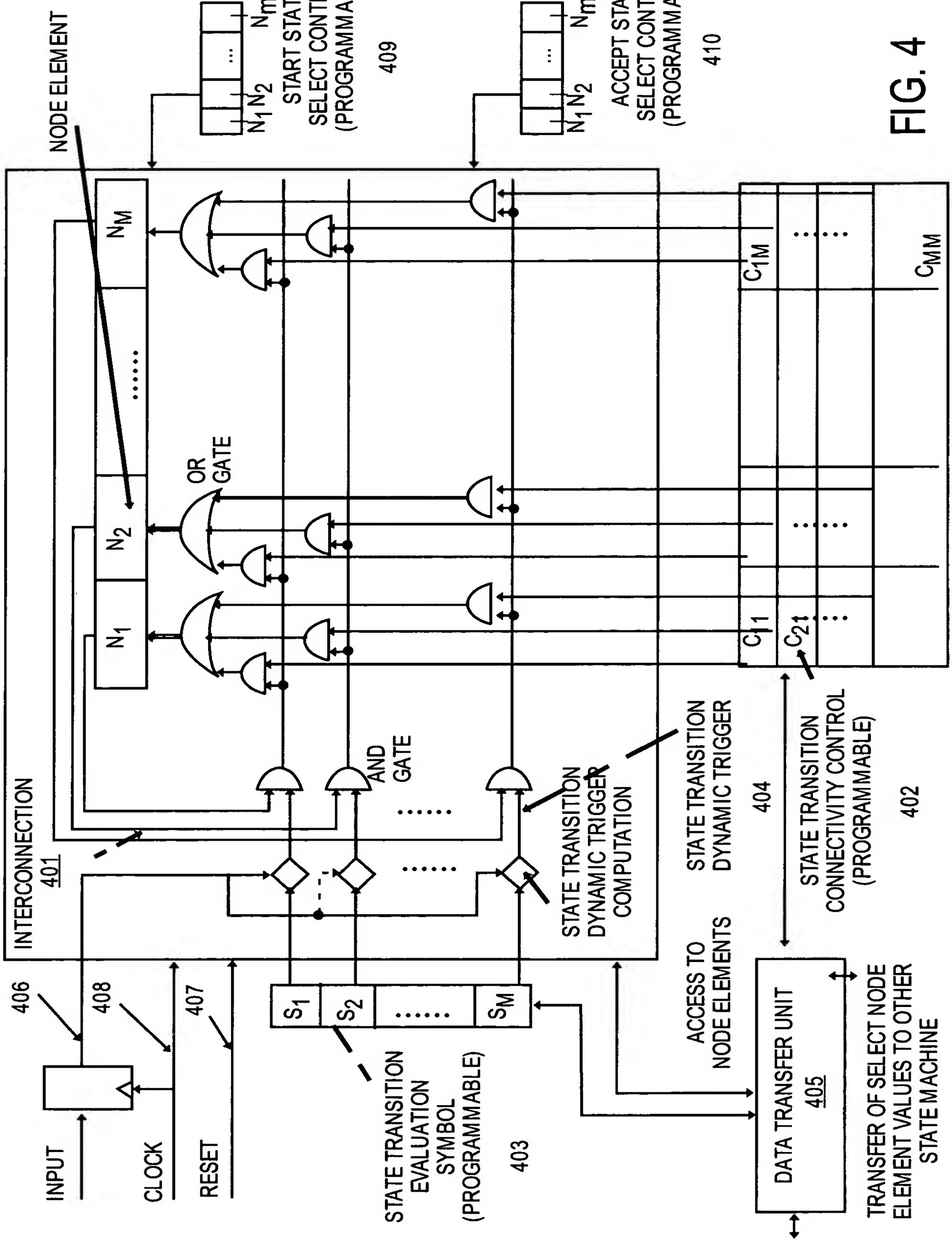

INTERCONNECTION
401
NODE ELEMENT
N_M
N_2
N_1
OR GATE
AND GATE
$N_1 N_2$ ... N_m
START STATE SELECT CONTROL (PROGRAMMABLE)
409
$N_1 N_2$ ... N_m
ACCEPT STATE SELECT CONTROL (PROGRAMMABLE)
410
C_{1M}
C_{MM}
C_{11}
C_{21}
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION
STATE TRANSITION DYNAMIC TRIGGER
404
STATE TRANSITION CONNECTIVITY CONTROL (PROGRAMMABLE)
402
406
408
407
S_1 S_2 ..... S_M
STATE TRANSITION EVALUATION SYMBOL (PROGRAMMABLE)
403
ACCESS TO NODE ELEMENTS
DATA TRANSFER UNIT
405
INPUT
CLOCK
RESET
TRANSFER OF SELECT NODE ELEMENT VALUES TO OTHER STATE MACHINE

FIG. 4

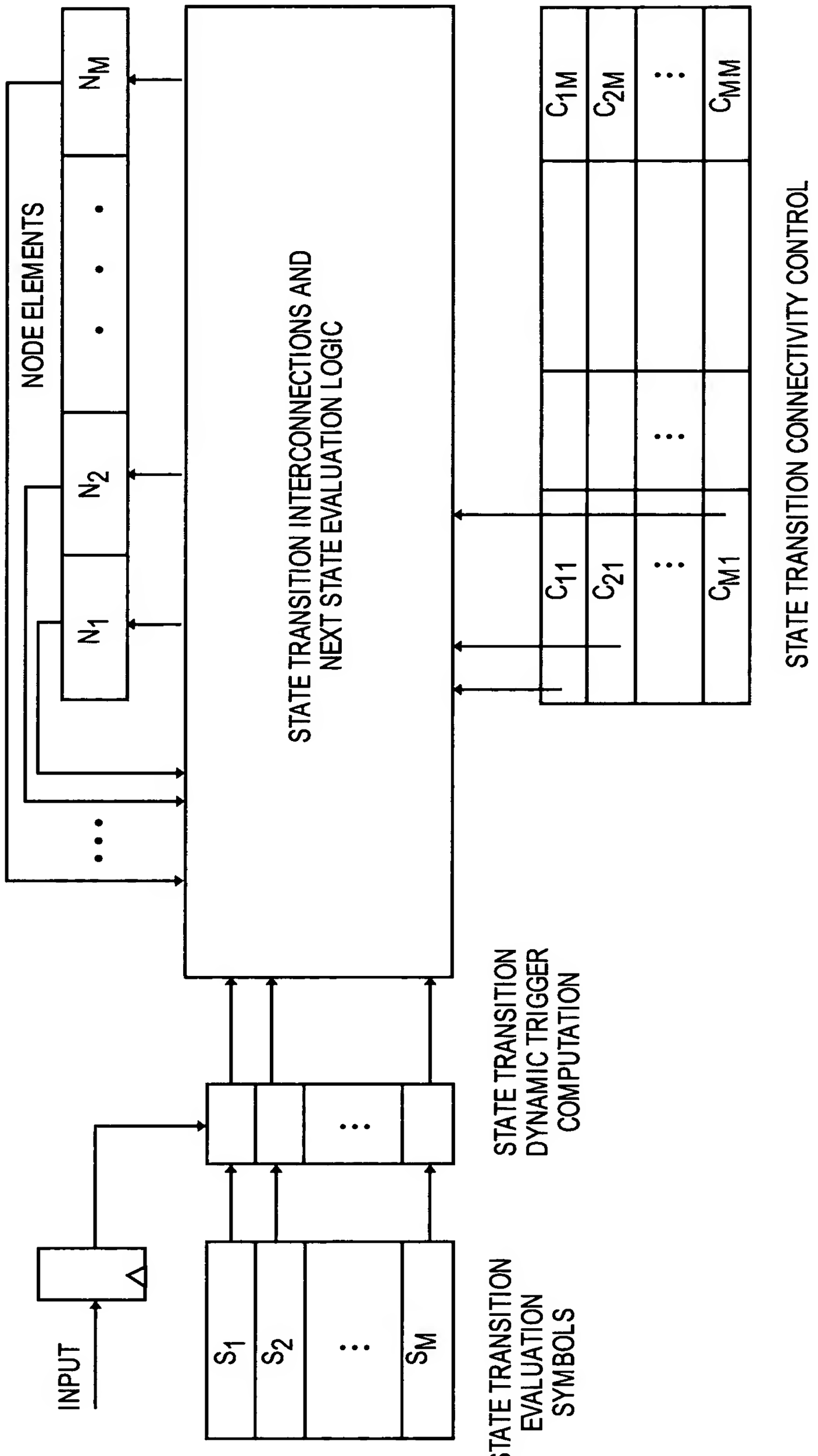

INPUT
Δ
S_1
S_2
S_M
STATE TRANSITION EVALUATION SYMBOLS
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION
N_1
N_2
N_M
NODE ELEMENTS
STATE TRANSITION INTERCONNECTIONS AND NEXT STATE EVALUATION LOGIC
C_{11}
C_{21}
C_{M1}
C_{1M}
C_{2M}
C_{MM}
STATE TRANSITION CONNECTIVITY CONTROL

FIG. 5

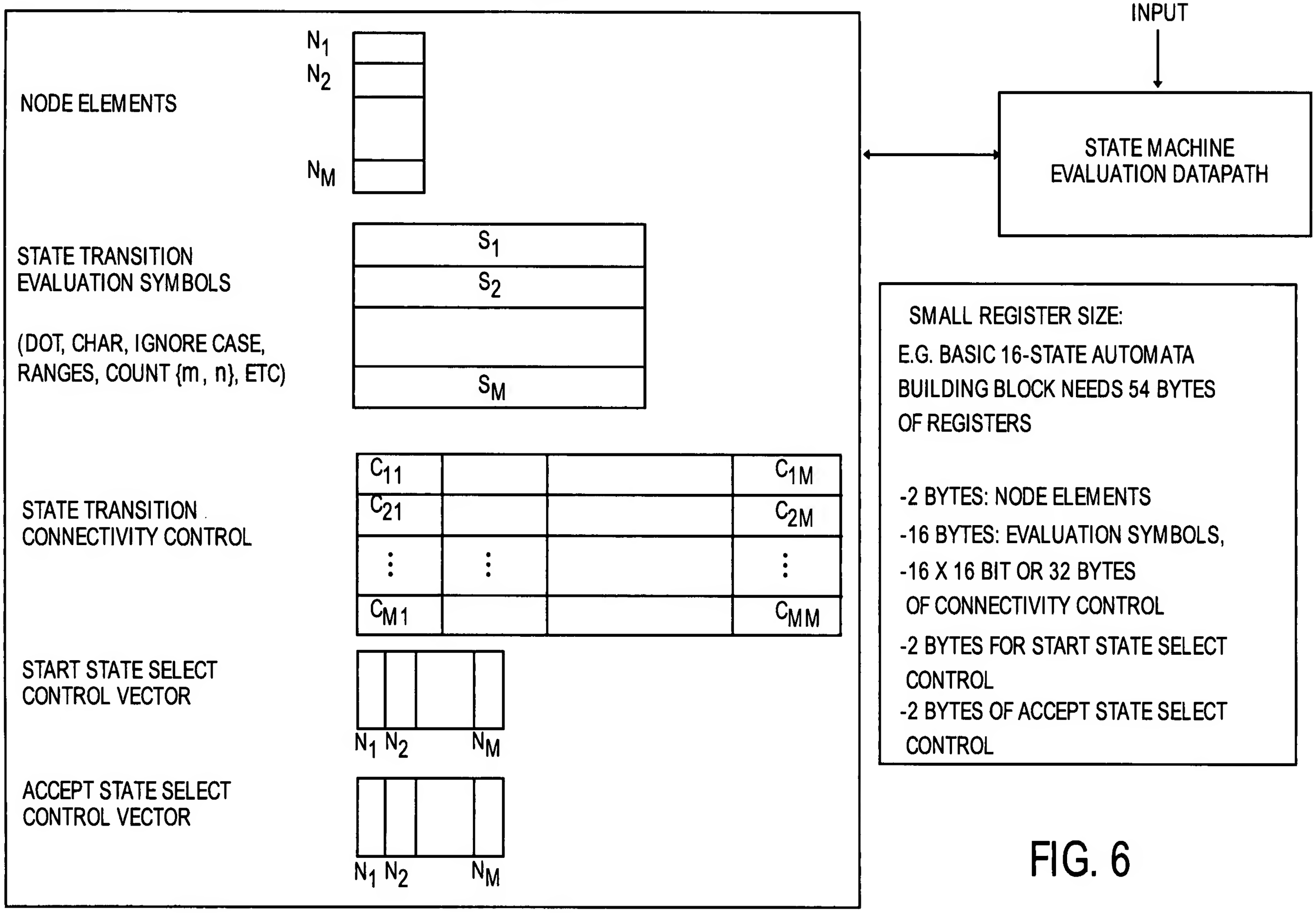

PROGRAMMABLE AUTOMATA REGISTERS (EXPRESSION REGISTERS)
NODE ELEMENTS
N_1
N_2
N_M
STATE TRANSITION EVALUATION SYMBOLS
(DOT, CHAR, IGNORE CASE, RANGES, COUNT {m, n}, ETC)
S_1
S_2
S_M
STATE TRANSITION CONNECTIVITY CONTROL
C_{11} C_{1M}
C_{21} C_{2M}
C_{M1} C_{MM}
START STATE SELECT CONTROL VECTOR
N_1 N_2 N_M
ACCEPT STATE SELECT CONTROL VECTOR
N_1 N_2 N_M
INPUT
STATE MACHINE EVALUATION DATAPATH
SMALL REGISTER SIZE:
E.G. BASIC 16-STATE AUTOMATA BUILDING BLOCK NEEDS 54 BYTES OF REGISTERS
-2 BYTES: NODE ELEMENTS
-16 BYTES: EVALUATION SYMBOLS,
-16 X 16 BIT OR 32 BYTES OF CONNECTIVITY CONTROL
-2 BYTES FOR START STATE SELECT CONTROL
-2 BYTES OF ACCEPT STATE SELECT CONTROL

FIG. 6

- SIMPLE REGULAR STRUCTURE ENABLES A HIGH DENSITY → DENSE ARRAY OF MULTIPLE TILES
- SEVERAL THOUSANDS OF AUTOMATA (ORGANIZED AS MULTIPLE ROWS OF TILES) CAN FIT ON A SINGLE DIE ON 0.13u TECHNOLOGY

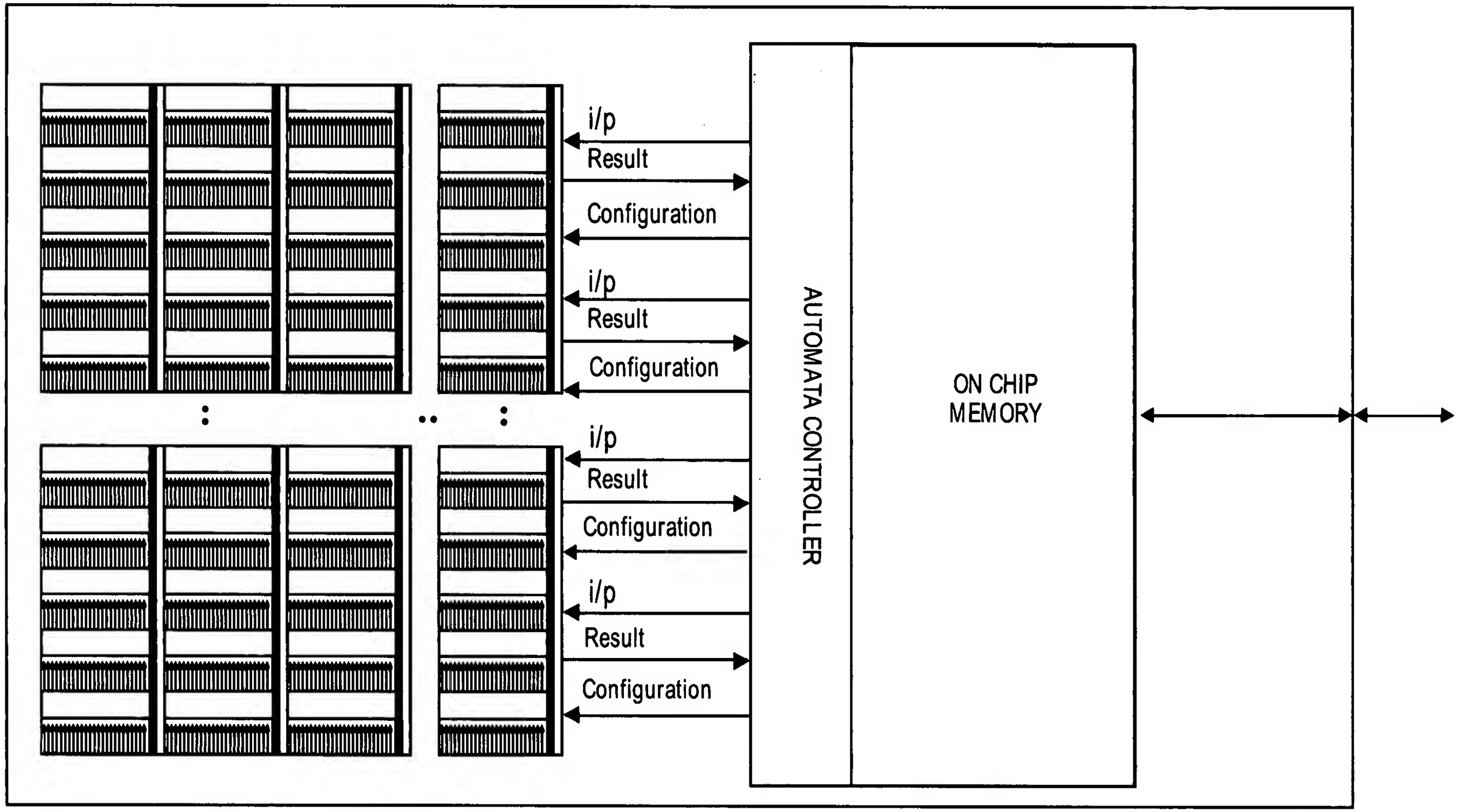


FIG. 7

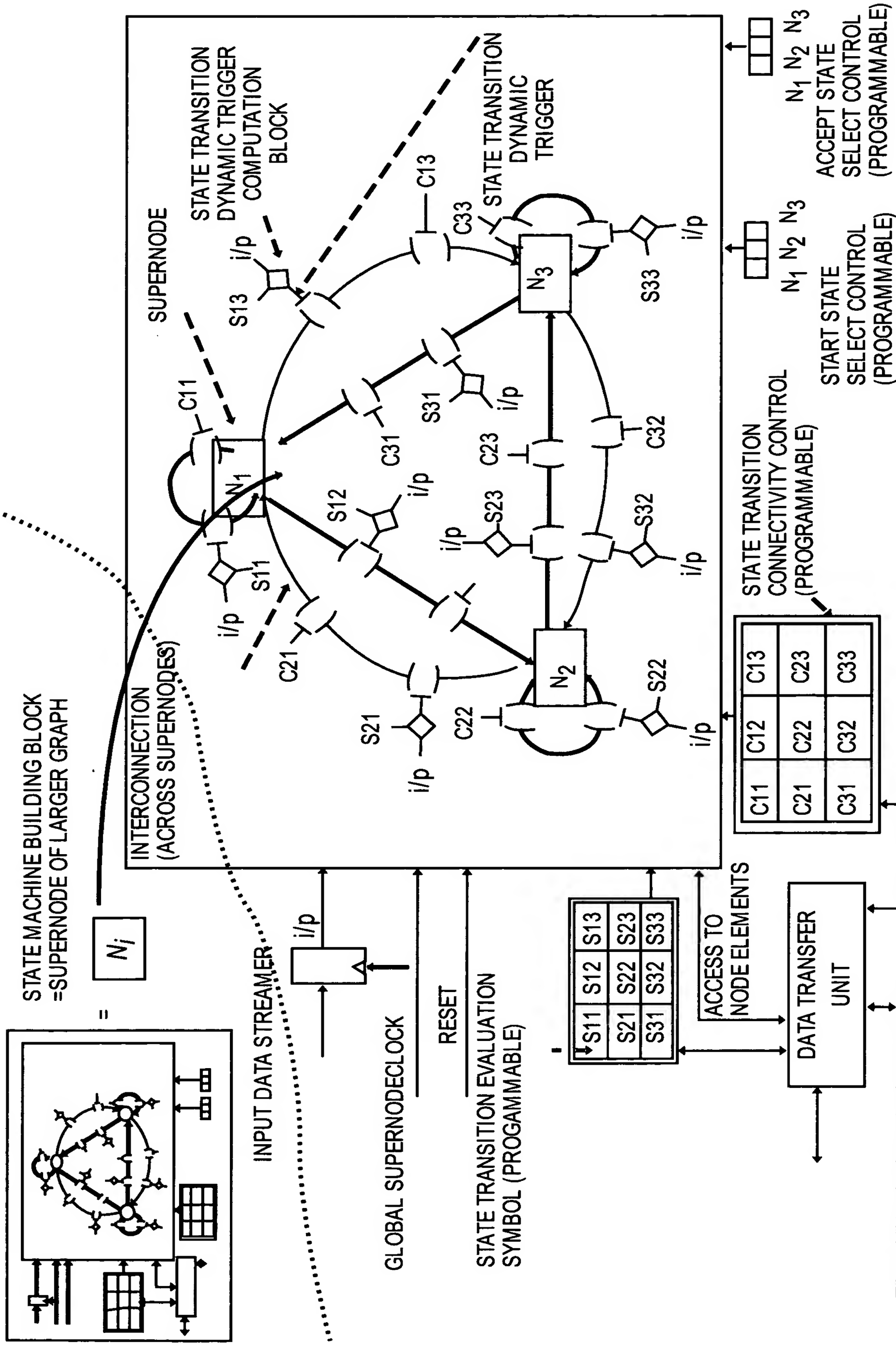
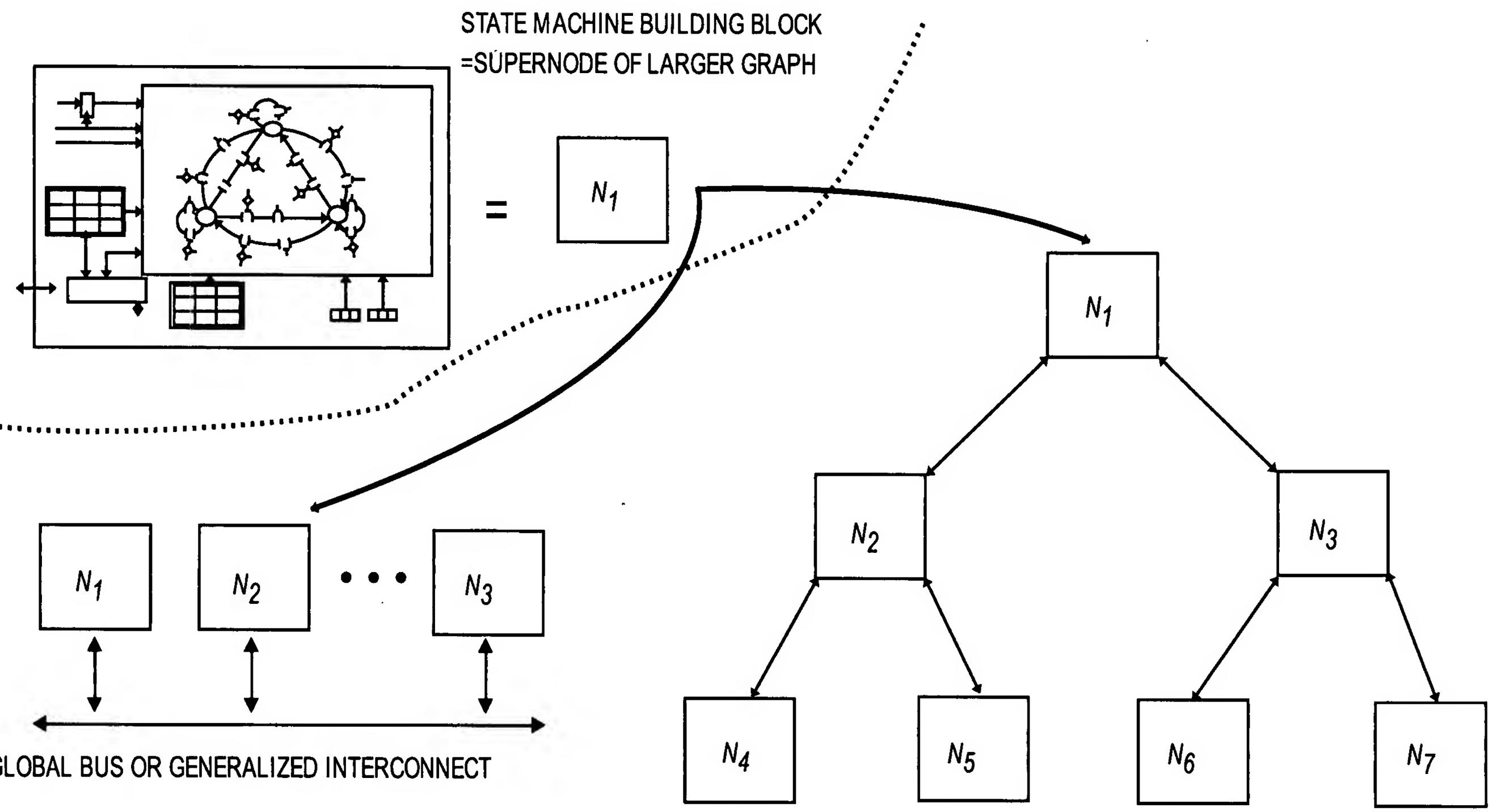

STATE MACHINE BUILDING BLOCK
=SUPERNODE OF LARGER GRAPH
N_i
=
SUPERNODE
STATE TRANSITION DYNAMIC TRIGGER COMPUTATION BLOCK
INTERCONNECTION (ACROSS SUPERNODES)
N_1
N_2
N_3
C11
C21
C31
C12
C22
C32
C13
C23
C33
S11
S21
S31
S12
S22
S32
S13
S23
S33
i/p
STATE TRANSITION DYNAMIC TRIGGER
N_1 N_2 N_3
ACCEPT STATE SELECT CONTROL (PROGRAMMABLE)
N_1 N_2 N_3
START STATE SELECT CONTROL (PROGRAMMABLE)
STATE TRANSITION CONNECTIVITY CONTROL (PROGRAMMABLE)
C11 C12 C13
C21 C22 C23
C31 C32 C33
S11 S12 S13
S21 S22 S23
S31 S32 S33
INPUT DATA STREAMER
GLOBAL SUPERNODECLOCK
RESET
STATE TRANSITION EVALUATION SYMBOL (PROGAMMABLE)
ACCESS TO NODE ELEMENTS
DATA TRANSFER UNIT
TRANSFER OF SELECT SUPERNODE VALUES TO OTHER STATE MACHINE

FIG. 8A

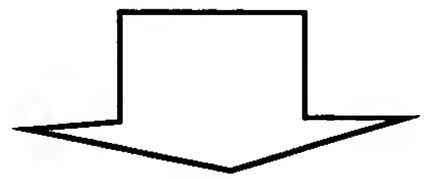


LARGER STATE MACHINE REALIZED VIA MULTIPLE STATE MACHINE BUILDING BLOCKS ON A GENERAL INTERCONNECT

LARGER STATE MACHINE REALIZED VIA MULTIPLE STATE MACHINE BUILDING BLOCKS ORGANIZED AS A TREE

FIG. 8B

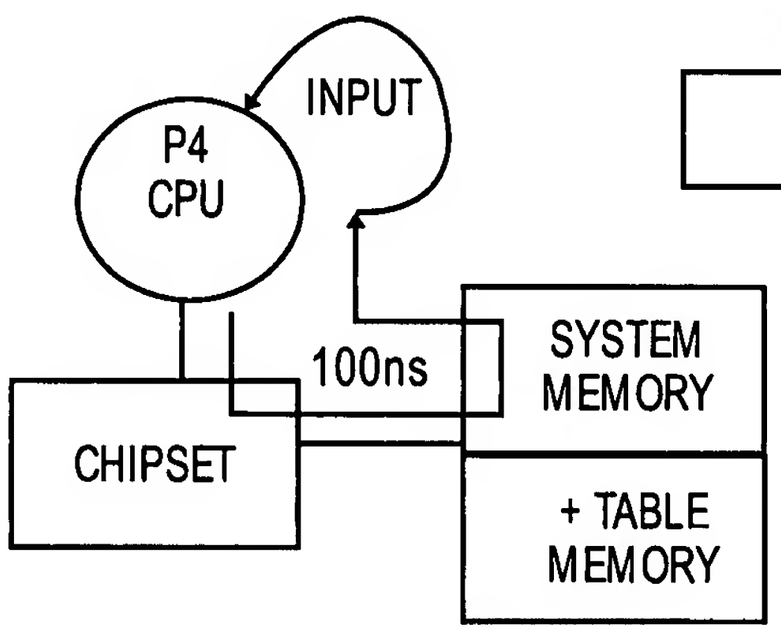
PROPERTIES OF DFA AND NFA TECHNIQUES USED ON CONVENTIONAL MICROPROCESSORS	STORAGE: BOUND ON # OF STATES (FOR R CHARACTERS)	EVALUATION TIME (FOR N BYTES) [ORDER OF]
DETERMINISTIC FINITE STATE AUTOMATA OR DFA RUNNING ON A GP CPU	2^R (NEEDS VERY LARGE MEMORY)	N MEMORY ACCESS CYCLES (~100ns)
NON-DETERMINISTIC FINITE STATE AUTOMATA OR NFA RUNNING ON A GP CPU	R	R * N CPU CACHE+BRANCH CYCLES (~4ns)



NON-DETERMINISTIC FINITE STATE AUTOMATA OR NFA RUNNING ON THE APPARATUS	R	N TIGHT ON CHIP STATE TRANSITION CYCLE (~1 ns)

FIG. 9A
(PRIOR ART)

CPU WALKING DFA TABLE IN DRAM

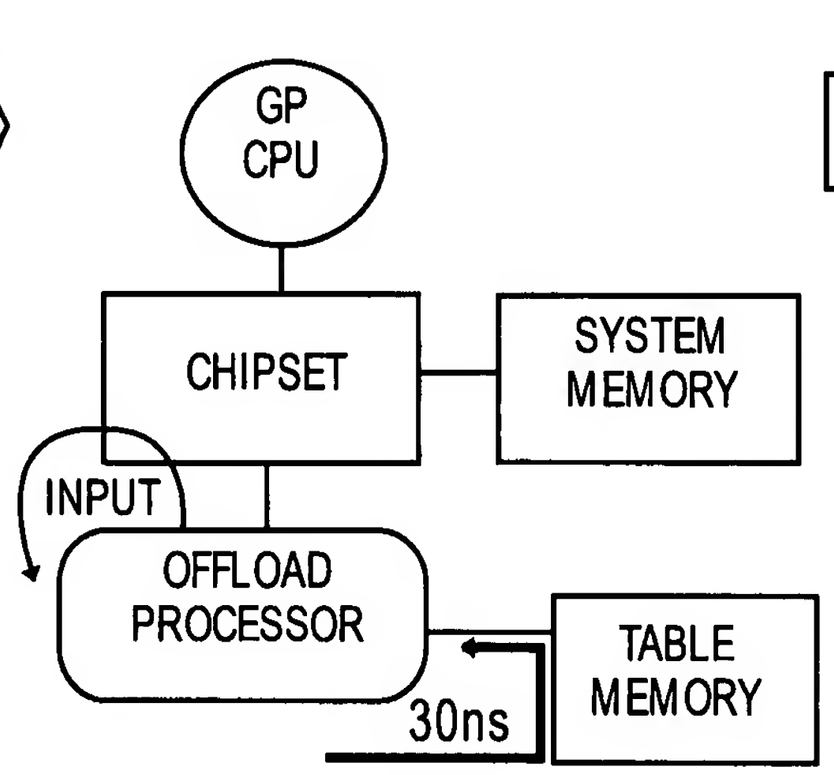


PERF ON REs ON EVERY BYTE

1000s OF REs @ 100 Mbps

GIGABYTES OF MEMORY

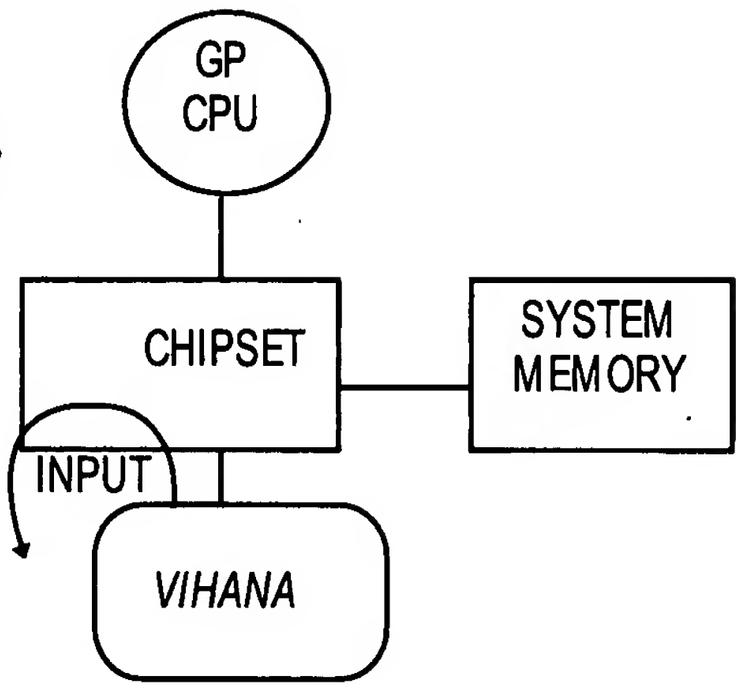
COPROCESSOR CLOSER TO TABLE IN SRAM



100s OF REs @ 280 Mbps

100s OF MBs OF SRAM

REGULAR EXPRESSION CO-PROCESSOR USING EXEMPLARY STATE MACHINE ARCHITECTURE



1000s OF REs @ > 10Gbps

NO TABLE MEMORY NEEDED

TWO ORDERS OF MAGNITUDE SPEEDUP WITHOUT NEED FOR TABLE MEMORY

FIG. 9B